Integrated Circuit Design of CMOS Protection Circuitry for GaN DC-DC Converters

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Abstract*—This paper presents the design and simulation of integrated CMOS protection circuits suitable for gallium nitride (GaN) regulators. Considering the vulnerability of GaN devices under high-frequency conditions, three core protection modules are focused on: a high-speed hysteresis comparator as the general detection core, an under-voltage lockout (UVLO) circuit with a bandgap reference, and two short-circuit protection (SCP) schemes - one using resistance-based current detection with automatic recovery function, and the other using desaturation detection technology and integrating hidden time control to prevent false triggering. The simulation results show that the hysteresis comparator achieves a 120mV hysteresis window and a 3ns propagation delay; the UVLO circuit has a response time of ≤0.1μs and can maintain a stable reference voltage of 1.164V; the resistance detection SCP scheme has a response speed as fast as 45ns and supports automatic recovery; the de-saturation detection scheme sets a 0.1μs blanking time, and the over-current protection response is ≤ 0.1μs. This protection circuit constitutes a highly reliable and fast-response solution, which can effectively enhance the robustness of GaN DC-DC converters and is suitable for high-power density application scenarios.

Keywords — GaN; Buck Converter; Hysteresis Comparator; Under Voltage Lockout; Short Circuit Protection; CMOS circuit.

I. INTRODUCTION

With the expansion of applications in electric vehicles, data centers, and telecommunications for power supply systems, the demand for high-power-density and high-efficiency DC-DC converters is increasingly urgent [1]. A key technology in such applications is gallium nitride (GaN) power transistors, which feature extremely high switching performance and very low on-resistance, enabling operation at frequencies above 1 MHz and making it suitable for smaller-sized converters [2-5].

GaN devices are thinner, and thus more susceptible to electrical overstress compared to silicon metal-oxide-semiconductor field-effect transistors (Si MOSFETs) [6-8]. Their low threshold voltage and small gate oxide capacitance make them vulnerable to gate overvoltage [7], while the absence of a body diode and the small safe operating area (SOA) increase the probability of catastrophic breakdown in the event of overcurrent or short circuits [8-9]. In the 48V high-frequency operating environment, voltage spikes and current surges occur frequently, further exacerbating these vulnerability issues. Therefore, a protection circuit with high reliability and fast response capability is not only an ideal choice but also a necessary condition for ensuring the reliability of GaN-based power converters.

Existing research on integrated protection circuits has proposed various verified solutions, but each has trade-offs. For example, in under voltage lockout (UVLO), although using a Zener diode as a reference is simple and occupies a very small area [10], its output voltage is sensitive to temperature and process corners, which may cause threshold point deviations under different conditions. In overcurrent protection, direct detection techniques such as current sensing based on resistors are used, but they cause unnecessary power loss and require high-speed, high-gain comparators to detect small voltage drops [7]. On the other hand, desaturation detection achieves lossless detection by measuring the drain-source voltage (VDS) of the power switch, but this method is highly dependent on precisely controlled blanking time - the blanking time must ignore the normal VDS overshoot during the on period of the switch; otherwise, improper blanking time setting may lead to unnecessary false triggering or detection omissions [9], [11]. At MHz switching frequencies, these limitations in terms of interference resistance, accuracy, and timing control become particularly prominent.

To address these issues, this paper designs and analyzes the main CMOS protection circuit modules for GaN buck converters. It studies a high-speed hysteresis comparator as a universal detection core, an improved UVLO circuit, and two different short-circuit protection (SCP) schemes (one based on resistor detection and the other based on desaturation detection). The development of these modules aims to solve the specific limitations of existing methods, and the protection system constructed thereby has high reliability and fast response capability, providing a fundamental solution for the protection of GaN devices in high-frequency applications.

II. THE DESIGN OF PROTECTION CIRCUITRY

A. The Hysteresis Comparator Circuit

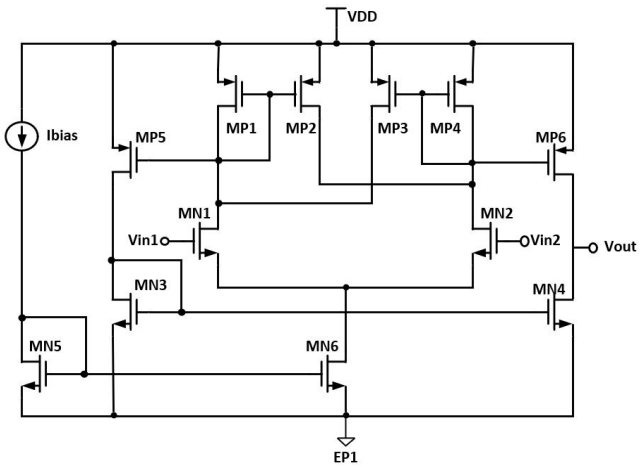

Fig.1 The structure of Hysteresis Comparator [12]

Building upon the hysteresis comparator configuration proposed by S. Nanda *et al.* [12], the hysteresis comparator aims to provide a stable and noise-resistant voltage detection function for protection systems. As shown in Figure 1, the circuit consists of three parts: a differential input stage, a positive feedback network, and an output buffer stage. The differential pair (MN1, MN2) is biased by a tail current source (MN6) and is used to compare two input voltages (Vin1, Vin2). The active load (MP1, MP4) converts the input current into a voltage signal. The output stage is composed of MP5, MP6, MN3, and MN4, which buffers the internal signal and achieves rail-to-rail output (VOUT) to drive subsequent logic circuits.

The key to achieving hysteresis lies in the cross-coupled transistor pair (MP2, MP3), which forms positive feedback between the output nodes, thereby generating two different switching thresholds. For example, when the input voltage Vin2 rises, the conduction of MN2 is enhanced, the drain current increases, and its drain voltage drops; at the same time, the current of MN1 decreases, and its drain voltage rises. Due to the positive feedback through the cross-coupled PMOS transistors (MP2, MP3), when the drain voltage of MN1 rises, the VSG of MP2 decreases, its pull-up capability weakens, causing the drain voltage of MN2 to drop, which in turn increases the VSG of MP3, enhances its pull-up capability, and further drives the drain voltage of MN1 to rise, forming a positive feedback. This positive feedback mechanism rapidly amplifies the differential voltage when the input voltage changes, causing the output level to flip quickly and generating a distinct hysteresis characteristic. This structure can effectively distinguish the trigger thresholds in the rising and falling directions, suppress false transitions caused by input noise, and ensure stable and reliable switching responses of the comparator in a noisy power supply environment [12].

B. The Under Voltage Lockout Circuit

Based on the research of R. L. Greenwel et al. [10], this paper proposes an improved under-voltage lockout circuit by replacing the traditional zener diode - reference source with a bandgap reference structure shown in Figure 2.

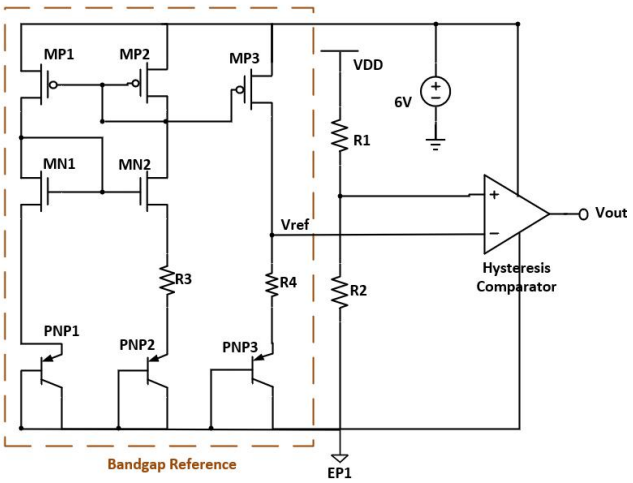

Fig.2 The Structure of Under Voltage Lockout

The bandgap reference module adopts a three-tube PNP structure, with the area ratio of the emitter junctions being 1:8:1. This structure generates a base-emitter voltage difference (ΔVBE) through the area difference, which is converted into a PTAT current by resistor R3. This current is mirrored to the output branch by current mirror MP3, and superimposed with the VBE voltage of PNP3. Since ΔVBE has a positive temperature coefficient while VBE has a negative temperature coefficient, by designing the resistance value ratio of R3 and R4, the two temperature coefficients are mutually compensated, ultimately generating a stable reference voltage VREF of approximately 1.2V at the output terminal.

The voltage detection part adopts the comparator structure with hysteresis feature proposed previously. Through the positive feedback mechanism, hysteresis characteristics are generated. The power supply voltage VDD is sampled through the resistor voltage divider network R1 and R2, and the sampled voltage is compared with the bandgap reference voltage VREF.

C. The Short Circuit Protection Circuits

a. Resistor Sensing Scheme

Based on the architecture proposed by R. L. Greenwell et al. [10], this paper proposes a resistor sensing scheme with automatic recovery function.

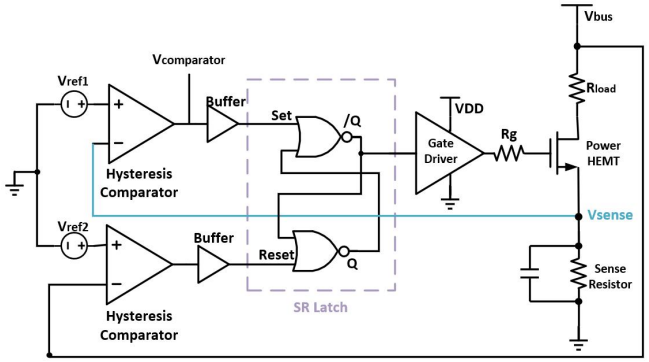

Fig.3 The Circuit Diagram of Resistor Sensing SCP

As shown in Figure 3, the circuit uses a 2 Ω sense resistor to continuously monitor the load current. The voltage drop across the sense resistor (Vsense) is compared with the preset reference voltage (Vref1) through a hysteresis comparator. When the system is operating normally, the sampling voltage is always below the threshold. Once an over-current or short circuit fault occurs, the voltage drop across the sense resistor exceeds the threshold of the comparator, and the fault signal output (Vcomparator) sets the SR latch, immediately turning off the gate driver and shutting off the main power switch, cutting off the fault current effectively.

The key improvement of this design lies in the automatic recovery mechanism based on the SR latch. After a fault occurs, the system continuously monitors the bus voltage (Vbus) through an independent voltage comparator (Vref2). Once the fault is eliminated, the system needs to meet two conditions to achieve automatic recovery: Vsense drops below the hysteresis threshold and Vbus returns to its normal range. Then, the generated reset signal clears the fault state of the SR latch, and the system automatically restarts.

This protection mechanism based on the SR latch ensures that the system only restarts when both current and voltage parameters have stably recovered, effectively avoiding the risk of false recovery under abnormal conditions.

b. De-saturation Scheme

The desaturation protection circuit provides an improved solution for overcurrent protection by monitoring the drain-source voltage (VDS) of the power switch transistor [10]. The core architecture consists of three key modules: the detection module, the blanking time module, and the logic control module, as shown in Figure 4.

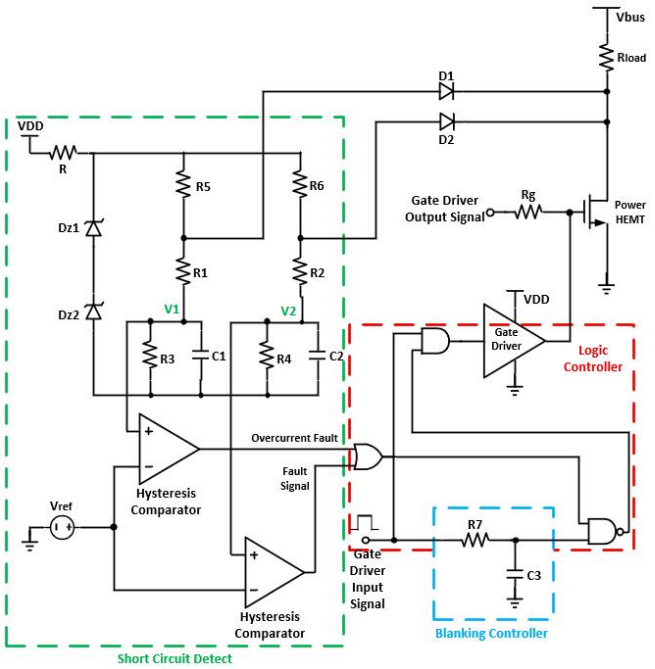

Fig.4 The Circuit Diagram of De-saturation SCP

This scheme employs a level-shifting network to sample the VDS of the high-side transistor through diodes D1 and D2 during the conduction period of the power switch transistor. When the power transistor is conducting normally, VDS remains at a low level, and the voltages at nodes V1 and V2 are below the comparator threshold (Vref), so the protection circuit does not act. In the event of an overcurrent, VDS rises, and capacitor C2 charges to cause the first comparator to output a short-circuit fault signal. If the short circuit persists, VDS further increases, and capacitor C1 charges to trigger the second comparator to output an overcurrent fault signal.

The core innovation of this design lies in the integration of a blanking time control circuit composed of resistor R7 and capacitor C3. When the Gate_Driver_Output_Signal (PWM) turns on the power switch transistor, the PWM generates a fixed-duration blanking pulse. During this period, the output of the de-saturation comparator is logically masked through a NAND gate, effectively ignoring the normal VDS overshoot that occurs during the transient conduction of the switch transistor.

After the blanking period ends, the protection circuit enters the working state. The fault signal is sent to the logic control unit composed of AND, OR, and NAND gates. This unit enables the fault detection function after the blanking time ends. Once a fault is confirmed, it immediately forces the gate driver to pull down the Gate_Driver_Output_Signal through logical combination, turning off the power switch transistor.

III. SIMULATION RESULTS

A. Hysteresis Comparator Circuit

Figure 5 presents the transient simulation results of the proposed hysteresis comparator under test conditions. The internal positive feedback hysteresis mechanism is implemented using NMOS (VTO = 0.7V, KP = 120 µ) and PMOS (VTO = -0.7V, KP = 50µ) transistors (These parameters are also applied to the subsequent simulations). The input configuration includes a fixed 2.5V reference voltage (Vin1) and a triangular waveform (Vin2) that scans from 0V to 5V with a period of 10 µs, corresponding to a frequency of 100kHz. The power rails are set at VDD = 4V and VSS = 1V.

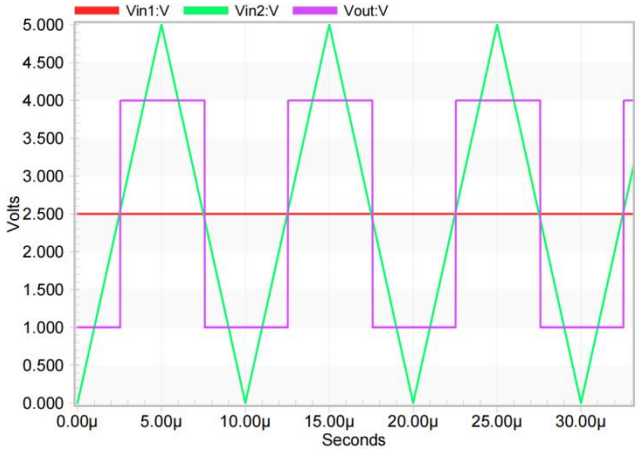

Fig.5 The Simulation Result of Hysteresis Comparator

The waveforms clearly show the triangular input signal Vin2 oscillating between 0V and 5V, while the output Vout exhibits precise square-wave switching behavior near 2.5us, 7.5us, 12.5us, and 17.5us.

This comparator has distinct hysteresis threshold characteristics: the upper switching threshold is 2.53V, the lower switching threshold is 2.41V, and the hysteresis window is approximately 120mV. This 120mV hysteresis band provides sufficient noise margin and effectively prevents output jitter in slow input transitions or noisy environments.

The output transitions demonstrate excellent dynamic performance: both the rise time (10% - 90%) and fall time (90% - 10%) are less than 5 ns, and the propagation delay from the threshold crossing point is approximately 3 ns, demonstrating the high-speed operation capability of the comparator.

Additionally, there is no overshoot or ringing in the output waveform, which also verifies its stability from another perspective. These characteristics make this comparator particularly suitable for precise voltage monitoring applications in power management systems.

B. *Under Voltage Lockout Circuit*

Figure 6 shows the transient simulation results of the proposed under-voltage lockout (UVLO) circuit. The Vdd power supply is a triangular waveform, dropping from 10V to 0V and then rising back to 10V within 20 us. The internal bandgap reference generates a stable voltage Vin2 of approximately 1.164V, unaffected by the change in Vdd.

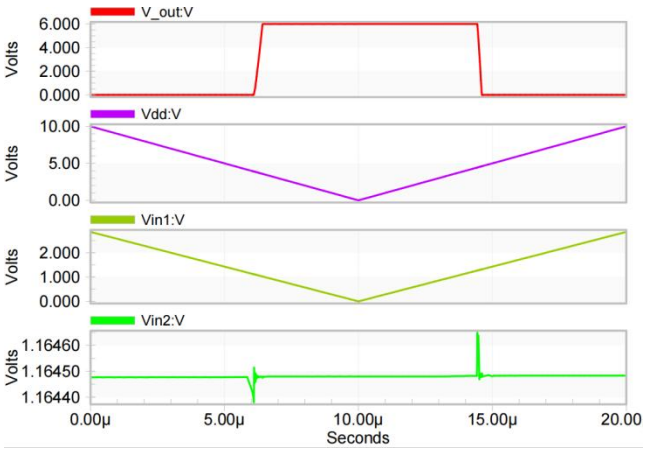

Fig.6 The Simulation Result of Under Voltage Lockout

The output voltage (Vout) reflects the expected UVLO function within 0.1us: when Vdd drops from the rated value, Vout remains at a low level until the first switching threshold is reached. At t ≈ 6.1 us, when Vdd drops to approximately 3.95V, the output rapidly jumps to a high level, indicating the under-voltage state. Conversely, during the Vdd recovery phase, at t ≈ 14.4 us and when Vdd rises to approximately 4.35V, the output switches back to a low level. The difference between the turn-off and turn-on thresholds forms a hysteresis window of approximately 400 mV, ensuring anti-interference capability and preventing output jitter during slow power supply changes.

It can be observed in the bandgap reference voltage Vin2 that transient spikes occur at the moment of comparator output switching. This phenomenon is due to the power coupling effect within the circuit. When the comparator output stage undergoes a state flip, the instantaneous large current generated will cause voltage disturbances in the power supply network. Since the bandgap reference circuit and the comparator share a 6V power, this disturbance is coupled to the reference output terminal through the power line, forming the observed voltage spike. This phenomenon is very common in single-chip integrated circuits, but because it has an extremely short duration, it does not affect the DC working characteristics of the circuit and the reliability of the lock threshold function.

C. *Short Circuit Protection Circuits*

a. Resistor Sensing Scheme

Figure 7 illustrates the transient response characteristics of the short-circuit protection circuit based on resistance sampling and hysteresis comparator. The circuit exhibits excellent rapid response capability when a fault occurs: when the sampling voltage V_sense exceeds the set threshold at t = 3.69 us, the comparator output V_comparator flips within nanosecond time, immediately triggering the protection logic to turn off the gate drive signal from 5V to a low level within 45 nanoseconds, achieving rapid isolation of the power switch tube.

This circuit has a complete self-recovery function. When the bus voltage V_bus drops and the sampling voltage falls below the reset threshold (t = 17.2 us), the reset signal is effectively activated, and the gate drive signal automatically returns to the 5V normal operating level. This dual-threshold hysteresis control mechanism ensures that the circuit can immediately return to normal operation after the fault is eliminated, without the need for external intervention.

The measured data confirm that this protection circuit has a hysteresis window of 120 mV. It can effectively suppress noise interference while ensuring the reliability of protection and recovery actions. The fast response time of 45 ns combined with the self-recovery feature makes it particularly suitable for power conversion systems that require high reliability protection.

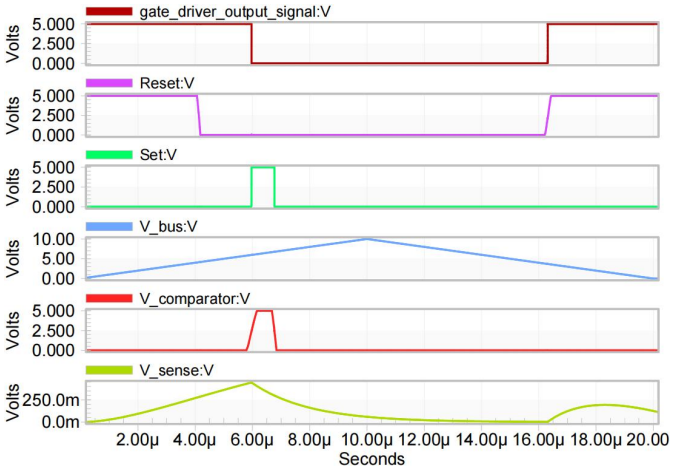

Fig.7 The Simulation Result of Resistor Sensing Scheme

b. De-saturation Scheme

Figure 8 shows the transient response characteristics of the over saturation protection circuit that integrates the extinction controller and the logic controller.

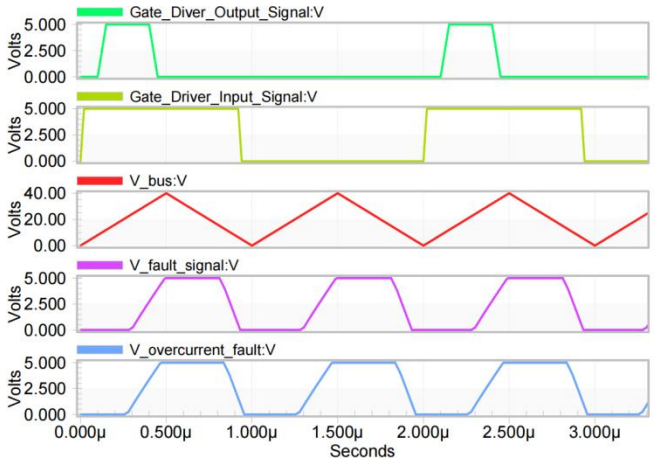

Fig.8 The Simulation Result of De-saturation Scheme

This circuit exhibits a key innovation during the initial turn-on stage: an approximately 100 ns long, precisely controllable extinction time generated by the RC network (R7, C3). Within the first 0.1 μs after the rising edge of the Gate_Driver_Input_Signal, the Gate_Driver_Output_Signal is forcibly maintained at 0V, effectively shielding the V_bus voltage spikes caused by the Miller effect during the normal turn-on process of the power switch tube, and fundamentally preventing incorrect triggering.

After the extinction time is over, the digital logic gate network takes over the control, and the gate driver output becomes a high level, allowing the power tube to conduct normally. At $t \approx 0.148$ μs, the bus voltage V_bus rises sharply and exceeds 25 V, which exceeds the internal set de-saturation protection threshold, thereby triggering the short circuit protection mechanism. At this time, the fault detection comparator rapidly flips, and both the V_fault_signal and the V_overcurrent_fault signals jump from a low level to a high level (5V). This fault state immediately causes the output of the logic control circuit based on NAND and AND gates to become a low level, thereby pulling the gate driver signal low and quickly and forcibly turning off the power switch tube within less than 0.1 μs, achieving reliable fault isolation.

In addition, the measurement results confirm that when the Gate_Driver_Input_Signal is zero, the output of the logic gate will remain at a low level continuously, ensuring that the power tube is in a safe off state.

IV. CONCLUSIONS

This paper designs multiple CMOS protection circuits suitable for gallium nitride (GaN) buck converters, and verifies it through simulation. The proposed hysteresis comparator achieves precise rail-to-rail voltage detection functionality, with a hysteresis window of 120mV and a propagation delay of approximately 3ns. It can be widely applied in subsequent protection circuits. The under-voltage lockout (UVLO) circuit demonstrates reliable operation performance within 0.1us, and can maintain a stable reference voltage of 1.164V. In terms of overcurrent protection, the overcurrent response time of the resistance detection-based scheme is 45ns, and it has automatic recovery capability; while the over-saturation detection scheme effectively avoids false triggering through a 0.1us blanking time control, and achieves a protection response within 0.1us.

The simulation results show that this circuit exhibits excellent performance in terms of response speed, anti-interference ability, and working stability. These protection circuits jointly solve the key reliability problems in high-frequency GaN converters, making them highly suitable for practical high-frequency power supply applications.

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